E-paper Module Specification

Module No.: SDE0368NQW-52

□ : APPROVAL FOR SPECIFICATION. □ : APPROVAL FOR SAMPLE

For Customer's Acceptance:

Approved By	Comment

Sunshine Display:

PREPARED	CHECKED	VERIFIED BY QA DEPT	VERIFIED BY R&D DEPT
Bob			

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REVISION RECORD

Rev No.	Rev date	Contents	Remarks
0.1	20260701	First release	Preliminary

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1 General Description

SDE0368NQW-52 is an Active Matrix Electrophoretic Display(AM EPD), with interface and a reference system design. The 3.68" active area contains 528x792 pixels. The module is a TFT-array driving electrophoretic display, with integrated circuits including gate buffer, source buffer, MCU interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2 Features

- 528x792 pixels display
- White reflectance above 30%
- Contrast ratio above 8:1
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Ultra Low current deep sleep mode
- On chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I^2C signal master interface to read external temperature sensor

3 Application

Electronic Shelf Label System

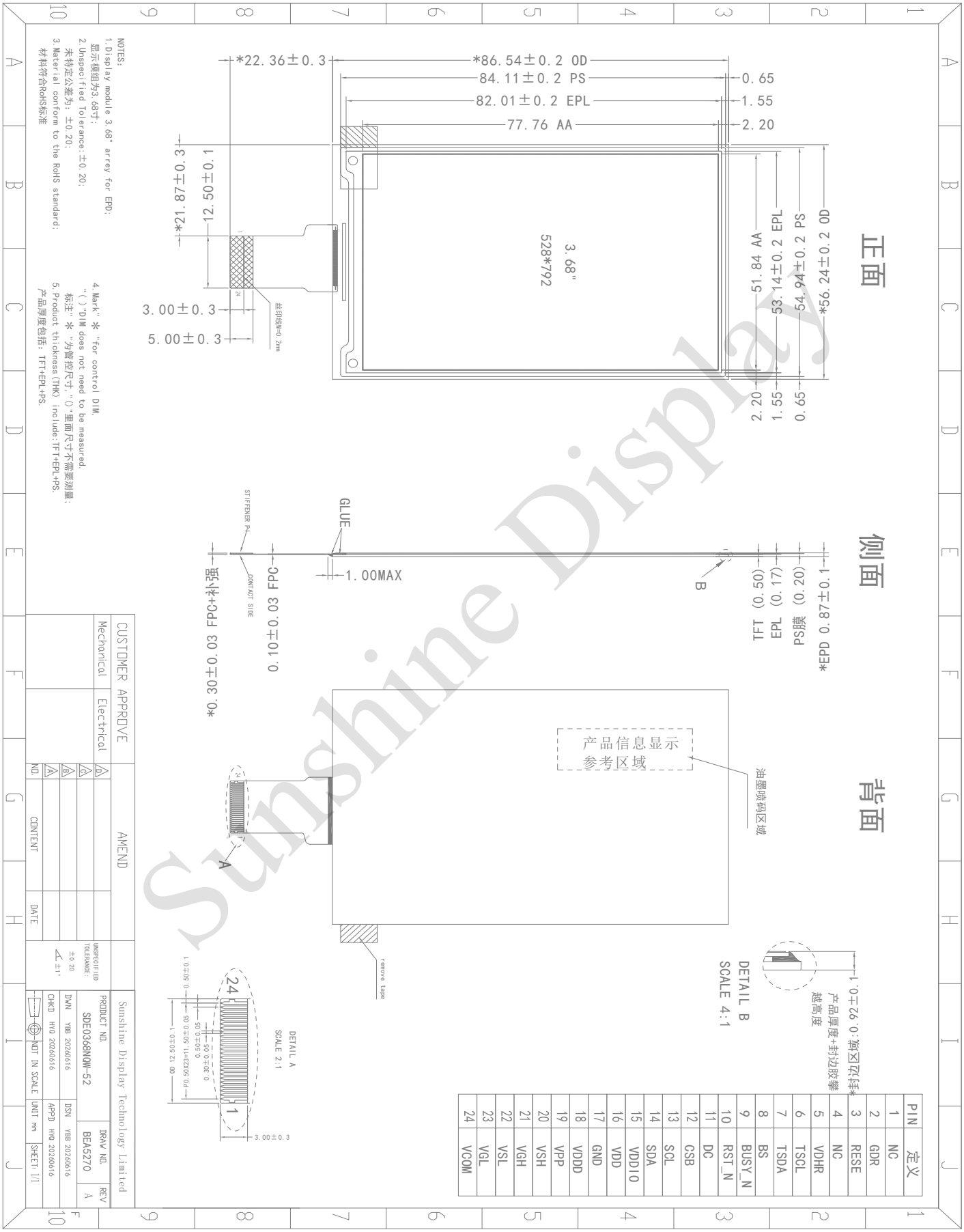
4 Mechanical Specification

4.1 Dimension

Parameter	Specifications	Unit
Screen Size	3.68	Inch
Display Resolution	528(H)×792(V)	Pixel
Active Area	51.84(H) × 77.76 (V)	mm
Pixel Pitch	94(H) ×94(V)	um(DPI 259)
Pixel Configuration	Rectangle	
Outline Dimension	56.24(H) × 86.54(V) ×0.87(D)	mm
Weight	TBD	g

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4.2 Mechanical Drawing of EPD Module



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5 Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC		Do not connect with other NC pins	
5	VDHR	C	Positive Source driving voltage 1	
6	TSCL	O	I^2C Interface to digital temperature sensor Clock pin	NC if not use
7	TSDA	I/O	I^2C Interface to digital temperature sensor Data pin	NC if not use
8	BS	I	Bus Interface selection pin	Note 5-4
9	BUSYN	O	Busy state output pin	Note 5-3
10	RSTN	I	Reset signal input. Active Low.	
11	D/C	I	Data /Command control pin	Note 5-2
12	CSB	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins	
16	VDD	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDDD	C	Core logic power pin VDDD can be regulated internally from VDD. A capacitor should be connected between VDDD and VSS under all circumstances	
19	VPP	P	Power Supply for OTP Programming	NC if not use
20	VSH	C	Positive Source driving voltage 2	
21	VGH	C	Positive Gate driving voltage	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Negative Gate driving voltage	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/Output), P = Power Pin, C = Capacitor Pin

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Note 5-1: This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CSB is pulled LOW.

Note 5-2: This pin is Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at D1 will be interpreted as data. When the pin is pulled LOW, the data at D1 will be interpreted as command.

Note 5-3: This pin is Busy state output pin. When Busy is Low, the operation of chip should not be interrupted, command should not be sent, e.g., The chip would put Busy pin Low when

- Outputting display waveform
- Programming with OTP
- Communicating with digital temperature sensor Note

5-4: Bus interface selection pin

BS State	MCU Interface
L	4-lines serial peripheral interface(SPI)
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6 Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{dd}	-0.3 to 6V	V
Logic Input voltage	V_{IN}	-0.3 to V_{ddio} +0.3	V
Logic Output voltage	V_{OUT}	-0.5 to V_{dd} +0.5	V

Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VDD=3.0V, T_{OPR} =25ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Logic supply voltage	V_{Vddio}	-	VDD	2.8	3.0	3.6	V
High level input voltage	V_{IH}	-	-	0.8 V_{dd}	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.2 V_{dd}	V
High level output voltage	V_{OH}	IOH = -100uA	-	0.8V_{dd}	-	-	V
Low level output voltage	V_{OL}	IOL = 100uA	-	-	-	0.2 V_{dd}	V
OTP Program voltage	V_{PP}	-	VPP	-	9.5	-	V
Typical power panel	P_{TYP}	-	-	-	TBD	TBD	mW
Deep sleep mode	P_{STPY}	-	-	-	3	-	uW
Typical operating current	Iopr_VDD	V_{dd} =3.0V-	-	-	TBD	TBD	mA

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Sleep mode current	Islp_VDD	VDD=3.0V DC/DC OFF No clock No output load Ram data retain	VDD	-	TBD	--	uA
Deep sleep mode current	IdslpVDD	VDD=3.0V DC/DC OFF No clock No output load Ram data not retain	VDD	-	1	--	uA
Operation temperature range	T_{OPR}	-	-	0	-	50	℃
Operation illuminance intensity	E	indoor only	-	-	-	2000	lux
Storage temperature range	T_{STG}	-	-	-25	-	60	℃
Storage relative humidity	RHst	-	-	30	-	60	%RH

Notes: 1. The typical power is measured with following transition:from horizontal 2 gray scale pattern to vertical 2 gray scale pattern. (Figure 10-2)

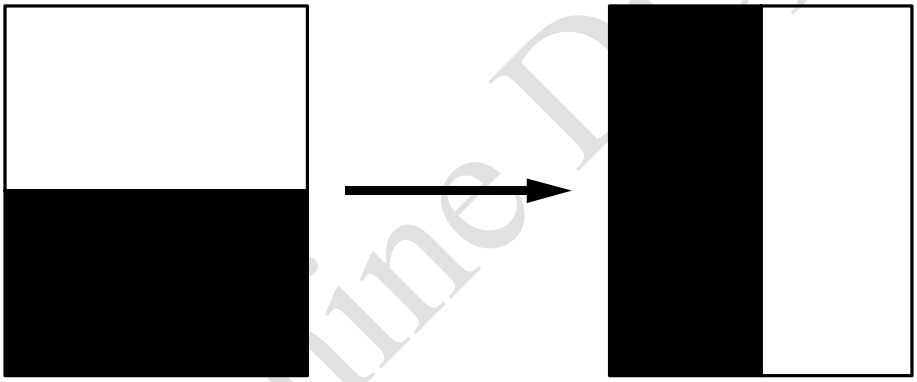


Figure 10-2 The typical power consumption measure pattern

2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by SID.

6.3 Panel DC Characteristics(Driver IC Internal Regulators)

The following specifications apply for: VSS=0V, VDD =3.0V, T_{OPR} =25ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCOM output voltage	VCOM	-	VCOM	-	-	-	V

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6.4 Panel AC Characteristics

6.4.1 MCU Interface Selection

MCU interface consist of 2 data/command pins and 3 control pins. The pin assignment at different interface mode is summarized in Table 10-4-1. Different MCU mode can be set by hardware selection on BS pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	**SDA**	**SCL**	**CSB**	**D/C**	**RSTN**
4-wire SPI	SDIN	SCLK	CSB	D/C	RSTN
3-wire SPI	SDIN	SCLK	CSB	L	RSTN

Table 10-4-1: MCU interface assignment under different bus interface mode

6.4.2 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCLK, serial data SDIN, D/C, CSB. In 4-wire SPI mode, SCL acts as SCLK, SDA acts as SDIN.

Function	CSB	D/C	SCLK
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

Table10-4-2: Control pins of 4-wire Serial interface

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

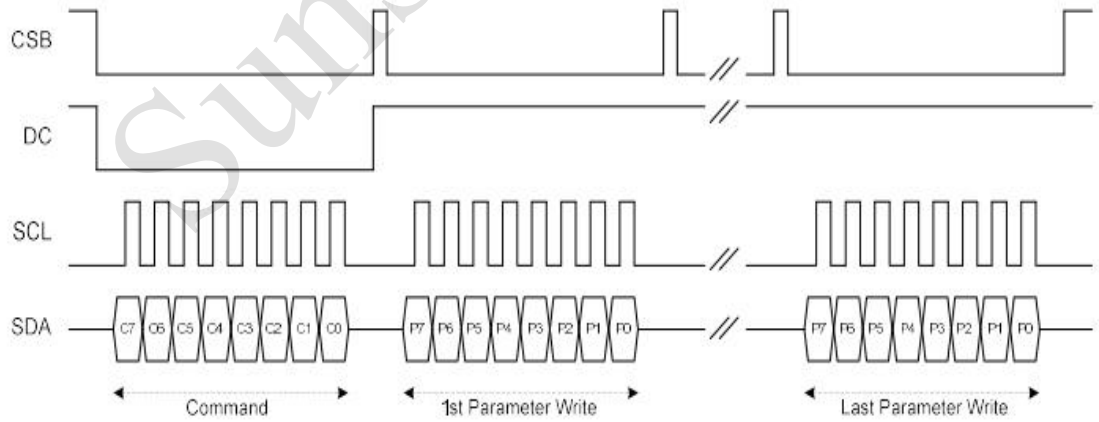


Figure: 4-wire SPI write operation

Figure 10-4-2: Write procedure in 4-wire SPI mode

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6.4.3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CSB. In 3-wire SPI mode, SCL acts as SCLK, SDA acts as SDIN.

The operation is similar to 4-wire serial interface while D/C pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C bit, D7 to D0 bit. The D/C bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C bit = 1) or the command register (D/C bit = 0).

Under serial mode, only write operations are allowed.

Function	CSB	D/C	SCLK
Write command	L	Tie	↑
Write data	L	Tie	↑

Note：↑ stands for rising edge of signal

Table 10-4-3: Control pins of 3-wire Serial interface

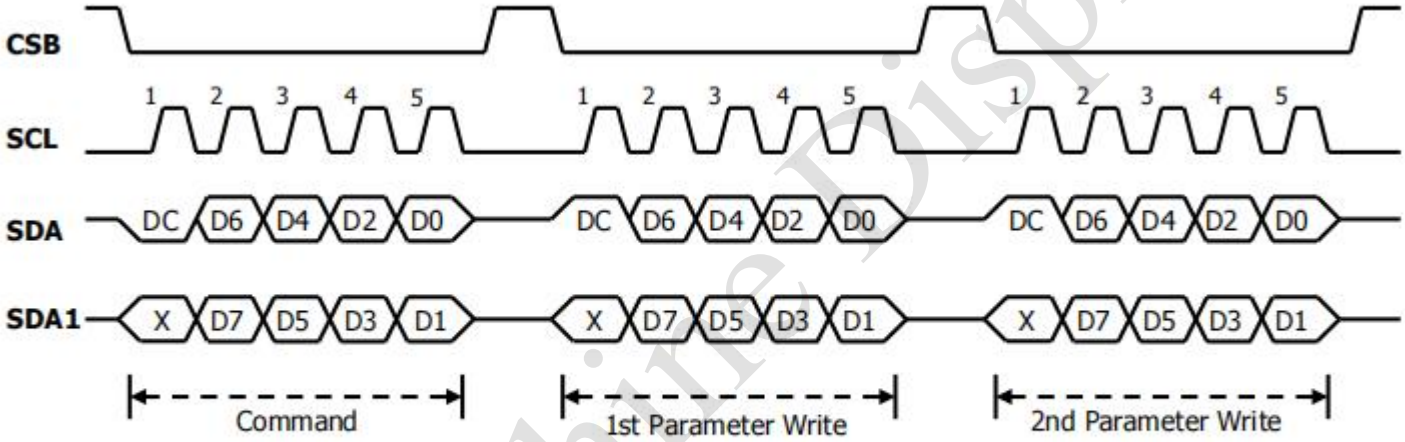


Figure: 3-wire dual SPI write operation

Figure 10-4-3: Read&Write procedure in 3-wire SPI mode

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6.4.4 Interface Timing

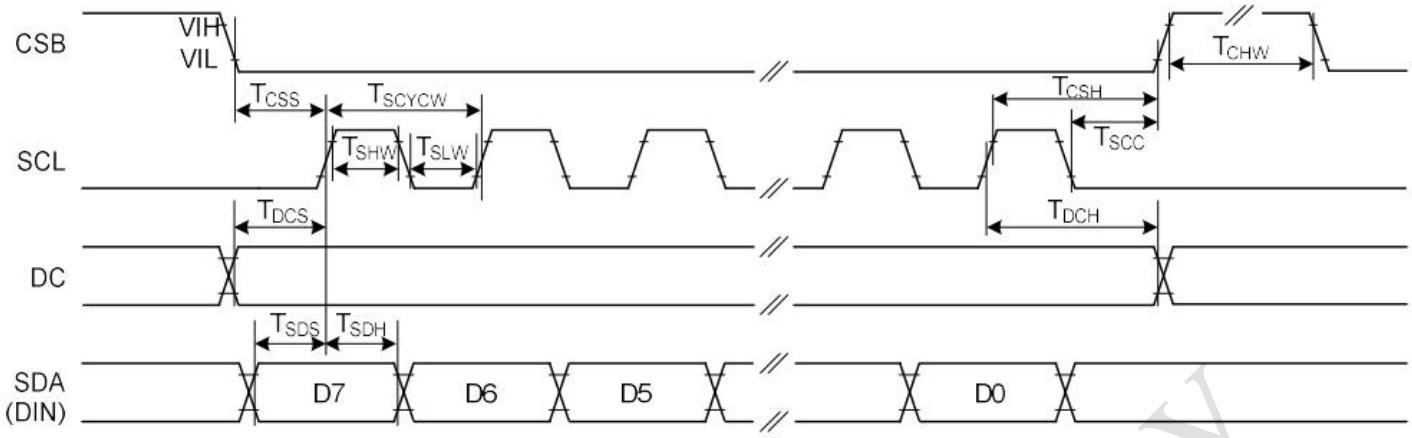


Figure: 4-wire Serial Interface Characteristics (Write mode)

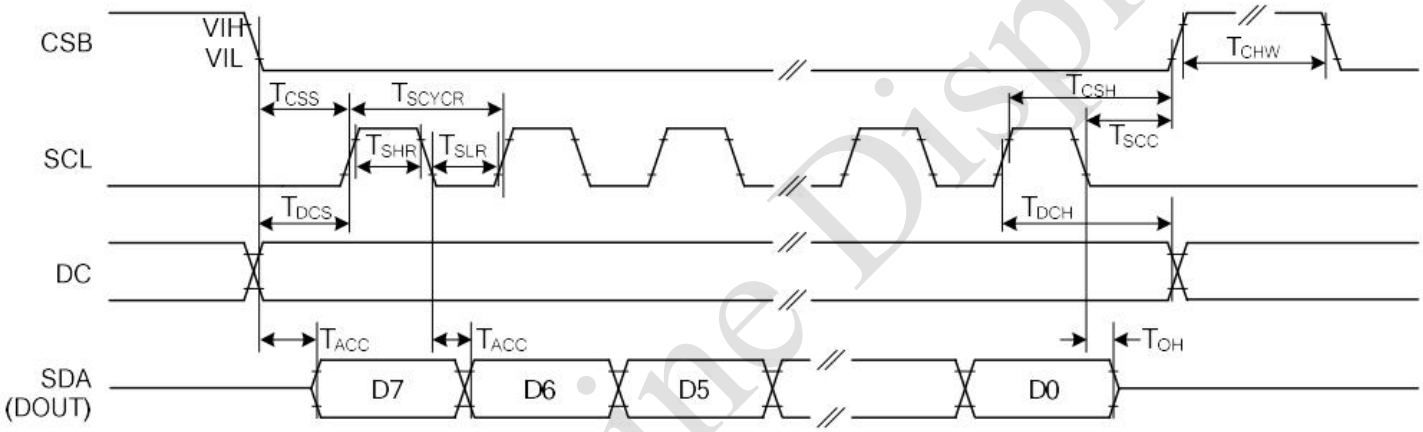


Figure: 4-wire Serial Interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100			ns
T_{SHW}		SCL "H" pulse width (Write)	35			ns
T_{SLW}		SCL "L" pulse width (Write)	35			ns
T_{SCYCR}		Serial clock cycle (Read)	350			ns
T_{SHR}		SCL "H" pulse width (Read)	175			ns
T_{SLR}		SCL "L" pulse width (Read)	175			ns
T_{DCS}	DC	DC setup time	30			ns
T_{DCH}		DC hold time	30			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			250	ns
T_{OH}		Output disable time	15			ns

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7 Optical Specification

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

Symbol	Parameter	Conditions	Values			Units	Notes
			Min.	Typ.	Max		
R	White Reflectivity	White	30	35	-	%	11-1
CR	Contrast Ratio		8:1	10:1	-	-	11-2
WhiteoL 24h	Reduce		-	≤4	-	-	-
$T_{update(5S)}$	Image update time	at 25 °C	-	TBD	-	ms	-
$T_{update(GC)}$	Image update time	at 25 °C	-	450	-	ms	-
$T_{update(DU)}$	Image update time	at 25 °C	-	900	-	ms	-

Notes: 11-1. Luminance meter: Eye-One Pro Spectrophotometer.

11-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

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8 Handling, Safety, and Environment Requirements

1. The EPD Panel / Module is manufactured from fragile materials such as glass and plastic, and may be broken or cracked if dropped. Please handle with care. Do not apply force such as bending or twisting to the EPD panel
2. The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
3. Do not apply pressure to the EPD panel in order to prevent damaging it
4. Do not connect or disconnect the interface connector while the EPD panel is in operation
5. Do not stack the EPD panels / Modules.
6. Keep the EPD Panel / Module in the specified environment and original packing boxes when storage in order to avoid scratching and keep original performance.
7. Do not disassemble or reassemble the EPD panel
8. Use a soft dry cloth without chemicals for cleaning. Please don't press hard for cleaning because the surface of the protection sheet film is very soft and without hard coating. This behavior would make dent or scratch on protection sheet
9. Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation
10. It's low temperature operation product. Please be mindful the temperature different to make frost or dew on the surface of EPD panel. Moisture may penetrate into the EPD panel because of frost or dew on surface of EPD panel, and makes EPD panel damage.
11. High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time. Please store the EPD panel in controllable environment of warehouse and original package. Without sunlight, without condensation a temperature range of 15ºC to 35ºC, and humidity from 30%RH to 60%RH.

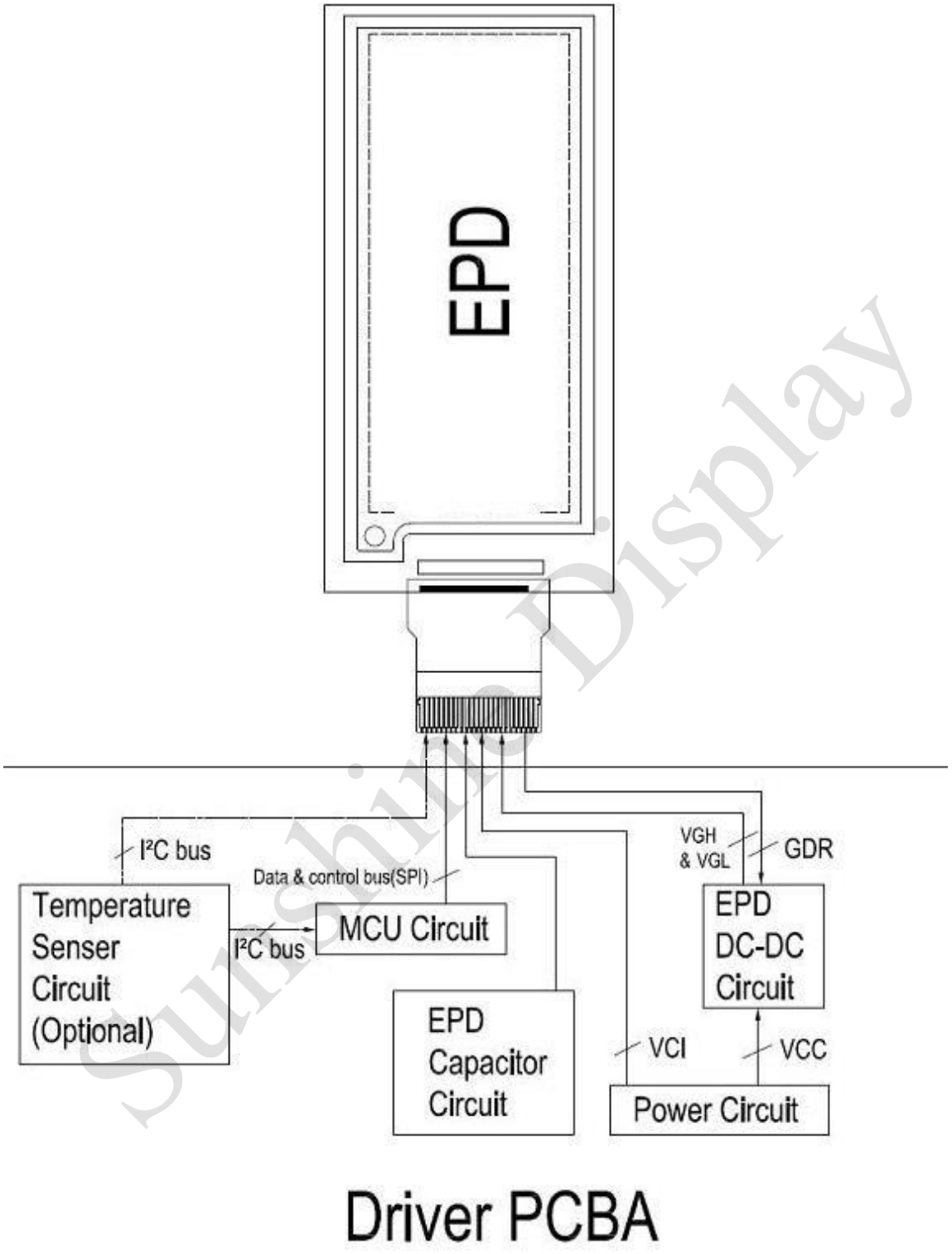
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9 Reliability Test

No.	Test	Condition	Method	Remark
1	High-Temperature Operation	T = +50°C, RH = 30% for 168 hrs	IEC 60 068-2-2Bp	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
2	Low-Temperature Operation	T = 0°C for 168 hrs	IEC 60 068-2-2Ab	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
3	High-Temperature Storage	T = +70°C, RH=23% for 168 hrs	IEC 60 068-2-2Bp	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
4	Low-Temperature Storage	T = -25°C for 168 hrs	IEC 60 068-2-1Ab	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
5	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% for 168 hrs	IEC 60 068-2-3CA	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
6	High Temperature, High-Humidity Storage	T = +60°C, RH=80% for 168hrs	IEC 60 068-2-3CA	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
7	ThermalShock	1 cycle:[-25°C 30min]→[+70 °C 30 min] : 100 cycles	IEC 60 068-2-14	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
8	Package Vibration	1.04G, Frequency: 10~500Hz Direction: X,Y,Z Duration: 1 hours in each direction	Full packed for shipment	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
9	Package Drop Impact	Drop from height of 122 cm on concrete surface. Drop sequence: 1 corner, 3edges, 6 faces One drop for each	Full packed for shipment	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
10	Electrostatic Effect (non-operating)	Machine model +/- 250V, 0Ω, 200pF	IEC 62179, IEC 62180	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.

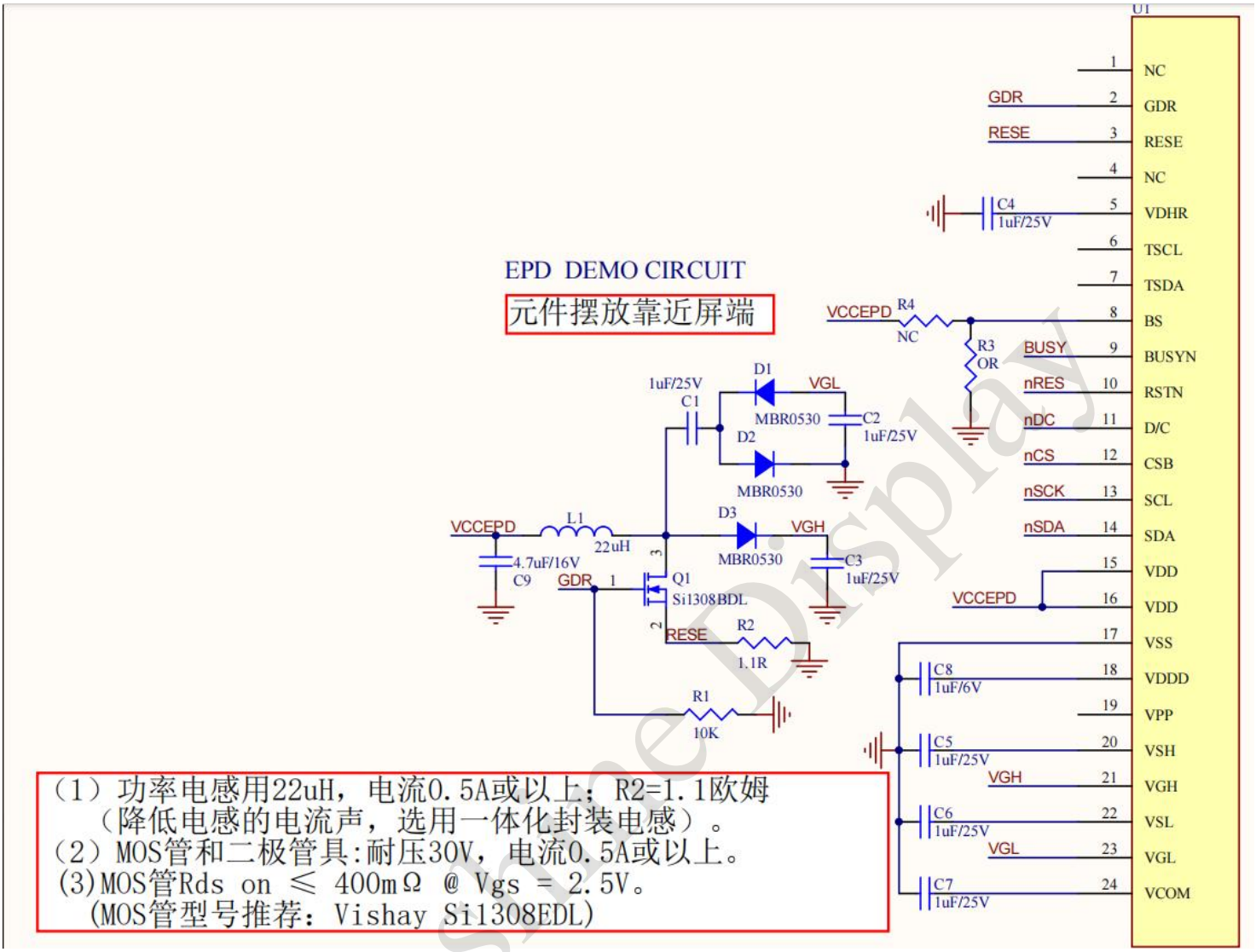
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10 Block Diagram



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11 Typical Application Circuit with SPI Interface



（1）功率电感用22uH，电流0.5A或以上；R2=1.1欧姆
（降低电感的电流声，选用一体化封装电感）。
（2）MOS管和二极管具:耐压30V，电流0.5A或以上。
(3)MOS管Rds on ≤ 400mΩ @ Vgs = 2.5V。
(MOS管型号推荐：Vishay Si1308EDL)

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12 Packaging

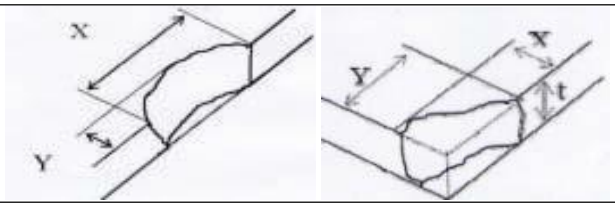
TBD

13 Mark and Bar Code Definition

TBD

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14. Point and line standard

<table>
<tr><th colspan="7">Shipment Inspection Standard</th></tr>
<tr><td colspan="7">Equipment： Electrical test fixture, Point gauge</td></tr>
<tr><td>Outline dimension</td><td>56.24(H) × 86.54(V) ×0.87(D)</td><td>Unit： ㎜</td><td>Part-A</td><td>Activearea</td><td>Part-B</td><td>Border area</td></tr>
<tr><td rowspan="2">Environment</td><td>Temperature</td><td>Humidity</td><td>Illuminance</td><td>Distance</td><td>Time</td><td>Angle</td></tr>
<tr><td>19℃～25℃</td><td>55%±5 %RH</td><td>600～1200Lux</td><td>300 ㎜</td><td>35Sec</td><td></td></tr>
<tr><td>Defect type</td><td>Inspection method</td><td colspan="2">Standard</td><td colspan="2">Part-A</td><td>Part-B</td></tr>
<tr><td rowspan="4">Spot</td><td rowspan="4">Electric Display</td><td colspan="2">D≤0.25 ㎜</td><td colspan="2">Ignore</td><td>Ignore</td></tr>
<tr><td colspan="2">0.25㎜＜D≤0.4 ㎜</td><td colspan="2">N≤4</td><td>Ignore</td></tr>
<tr><td colspan="2">0.4㎜＜D≤0.5 ㎜</td><td colspan="2">N≤2</td><td>Ignore</td></tr>
<tr><td colspan="2">D>0.5mm</td><td colspan="2">Not Allow</td><td></td></tr>
<tr><td>Display unwork</td><td>Electric Display</td><td colspan="2">Not Allow</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td>Display error</td><td>Electric Display</td><td colspan="2">Not Allow</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td rowspan="3">Scratch or line defect(include dirt)</td><td rowspan="3">Visual/Film card</td><td colspan="2">W≤0.15 ㎜</td><td colspan="2">Ignore</td><td>Ignore</td></tr>
<tr><td colspan="2">L≤3.0mm, 0.15＜W ≤0.3mm</td><td colspan="2">N≤2</td><td>Ignore</td></tr>
<tr><td colspan="2">L＞3. 0mm or W＞0.3㎜</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td rowspan="3">PS Bubble</td><td rowspan="3">Visual/Film card</td><td colspan="2">D≤0.3.mm</td><td colspan="2">Ignore</td><td>Ignore</td></tr>
<tr><td colspan="2">0.3mm≤D≤0.5mm</td><td colspan="2">N≤4</td><td>Ignore</td></tr>
<tr><td colspan="2">D＞0.5 mm</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td rowspan="2">Side Fragment</td><td rowspan="2">Visual/Film card</td><td colspan="5">X≤3mm,Y≤0.5mm, Do not affect the electrode circuit (Edge chipping)， N≤2
X≤2mm,Y≤2mm, Do not affect the electrode circuit((Corner chipping) ,N≤2</td></tr>
<tr><td colspan="5">
</td></tr>
<tr><td rowspan="3">Remark</td><td colspan="6">1.Cannot be defect & failure cause by appearance defect；</td></tr>
<tr><td colspan="6">2.Cannot be larger size cause by appearance defect；</td></tr>
<tr><td colspan="6">L=long W=wide D=point size N=Defects NO</td></tr>
</table>

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Note14-1：OQC inspection: One-time sampling plan for GB/T 2828.1-2012 , Inspection Level II, CR: AC/Re=0/1, MA=0.4,MI=1.0.

Note14-2：Spot define: That only can be seen under White State or Dark State defects

Note14-3：Any defect which is visible under gray pattern or transition process but invisible under black and white is disregarded.

Note14-4：Any defect must be judged by Optical Microscope.

Note14-5：Here is definition of the “Spot” and “Scratch or line defect”

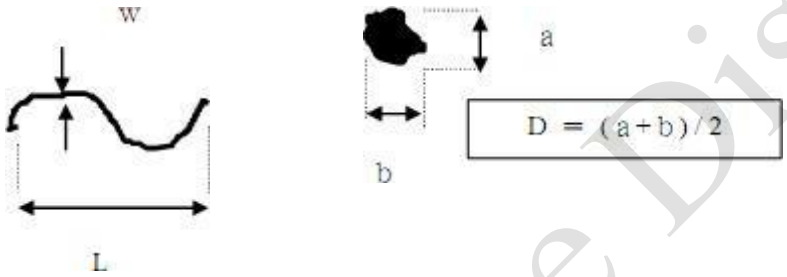
Spot: W>1/4L

Scratch or line defect :W ≤ 1/4L

Note14-6：Definition for L/W and D （major axis）

Note14-7：FPC bonding area pad doesn’t allowed visual inspection\

Note17-8：



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